Contact-less Topography of Yield-relevant Electrical Wafer Parameters

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Freiberg Instruments
Inline Metrology

scope

The worldwide rapidly growing progress in the development and manufacture of more and more sophisticated microelectronic semiconductor devices along with the necessity of high production yields call for powerful measurement tools in order to check quality parameters of the semiconductor materials used, e.g. wafers.

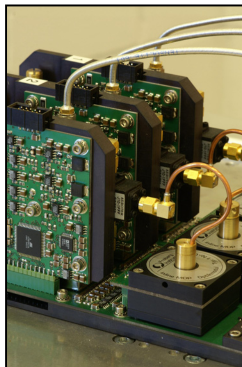
Although extreme efforts are made to push the production technology of wafers and devices along with the most advanced test facilities to the limits, it is simply a fact that always too many devices fail or do not meet specifications.

Performance of semiconductor devices depends fundamentally on key electrical parameters of the material such as mobility, lifetime, and diffusion length of minority charge carriers. However, only surprisingly little attention is paid so far to those dependencies along production lines. This is apparently also a consequence of so far insufficient metrology tools.

However, several breakthroughs were recently achieved. By the application of widely advanced microwave techniques it is now possible to measure the above mentioned electrical parameters 'without touching the wafer' with a so far unsurpassed combination of spatial resolution, sensitivity, and measurement speed.

equipment

- advanced inline metrology tools
- R&D tools



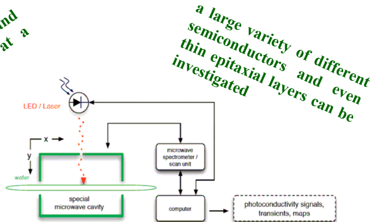
- investigation of semiconductor substrates, epitaxial layers, and chips
- topographic measurement of electrical parameters like diffusion length, lifetime, defect content and even drift mobility
- capability of device performance prediction by measurements with unprecedented sensitivity also at extremely low injection levels which give access to so far not accessible electrical material parameters

Innovative measurement system

measurement speed up to one wafer a second

allows for inline electrical parameter mapping such as: diffusion length, mobility, and lifetime, defect concentration, all together at a defect time.

a large variety of different semiconductors and even thin epitaxial layers can be investigated



Principle of the MDP and MD-PICTS setup

injection levels as typical for devices under normal operation – four orders of magnitude lower than used so far → access to so far not detectable defects

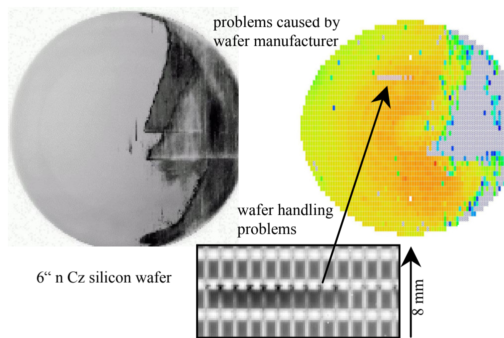
access to so far not measurable defects

advanced process control

The spatial resolution of the MDP topograms is only physically limited by the diffusion length of the generated carriers and not by limitations of the apparatus

wafer as obtained from manufacturer, MDP measurement at low injection levels

key parameter map of final devices (photodetectors). Grey: bad devices.

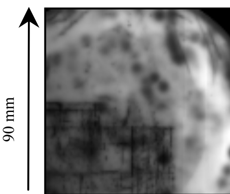


6" n Cz silicon wafer

device properties predicted by MDP-measurement of original wafer

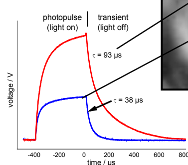
Yield limiting wafer inhomogeneities

float zone p- silicon as measured at extremly low injection levels

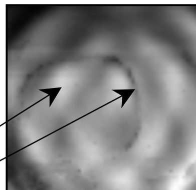


photoconductivity map

With the use of different wavelengths it is possible to distinguish between bulk and surface defects depending on the penetration depth.



epitaxial layer interface defects



photoconductivity map

So far not detectable yield limiting inhomogeneities and defects can be analyzed by MDP and MD-PICTS.

conclusion

- It could be verified that the production yield of final devices can be predicted by inspecting the original wafer, with speeds up to one second a wafer.
- It is possible to check the proper operation of individual processing procedures for each wafer. Also partially processed wafers can be measured.
- **Epitaxial layers** as used for device production can be topographically investigated with respect to device relevant electrical parameters.
- **Strained silicon** wafers can be measured in detail. The measurements provide a direct high resolution map of carrier mobility as a consequence of local strain. The spatial resolution is only physically limited by the diffusion length of the carriers. The carrier mobility turns out to be rather inhomogeneous over the wafer. In general it turned out that even the highest quality wafers and epitaxial layers available are considerably worse than they are believed to be, particularly in terms of homogeneity.

reference

[1] Topography of defect parameters on Si and GaAs, K. Dornich, B. Gründig-Wendrock, T. Hahn, J.R. Niklas, Adv. Eng. Mat. 2004, Vol. 6, No. 7

[2] Non destructive electrical defect characterisation and topography of silicon wafers and epitaxial layers, K. Dornich, T. Hahn, J.R. Niklas, MRS Symp. Proc., Vol. 864, 2005

[3] Contactless electrical defect characterisation of silicon by MD-PICTS, K. Dornich, K. Niemietz, Mt. Wagner, J.R. Niklas, Mat. Sci. Semi. Proc. 9, 2006, Elsevier, 241-245

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